

CLAIMS

1. A vertical trench-gate semiconductor device comprising a semiconductor body (2) having a top major surface (2a), and a plurality of trench-gates comprising trenches (6,6') extending into the semiconductor body from the top major surface with insulated gate electrodes (4) therein, the semiconductor body comprising source and drain regions (8,12) of a first conductivity type which are separated by a channel-accommodating region (10) of a second, opposite conductivity type adjacent the trench-gates, wherein the trench-gates extend in stripes, the source regions extend transversely between the trench-gates in stripes, projection (20) of the source stripes across the trench-gates defines intermediate trench portions (22) between the projected source stripes, and mutually spaced regions (14,14') of the second conductivity type are provided immediately below the intermediate trench portions (22) which are connected to source potential.

2. A device of Claim 1 wherein each spaced region (14,14') extends from the channel-accommodating region (10).

3. A device of Claim 2 wherein each spaced region (14,14') extends from the channel-accommodating region (10) on one side of the trench to meet the channel-accommodating region on the other side of the trench.

4. A device of any preceding Claim wherein the depth of each trench (6') oscillates along its length between depths above and below the lower boundary (10a) of the channel-accommodating region (10), such that the second conductivity type region that provides the channel-accommodating region extends periodically below the trench to form the spaced regions (14').

5. A method of manufacturing a vertical trench-gate transistor semiconductor device of Claim 4 comprising the steps of:

(a) forming a first mask (30) over the top major surface (2a) of the semiconductor body (2) defining a striped pattern of windows;

(b) introducing dopant of the first conductivity type for the source region (8) into the semiconductor body via the windows (32) of the first mask;

5 (c) forming a second mask (34) over the top major surface (2a) of the semiconductor body defining a striped pattern of windows (36) which extend transversely to the striped windows (32) of the first mask (30);

(d) introducing an etchant via the windows (36) of the second mask (34) to form trenches (6') in the semiconductor body (2), the etchant being selected
10 to etch both the semiconductor body and the first mask material, such that the resulting trenches are deeper than the lower boundary (100) of the channel-accommodating region (10) in the finished device within the lateral extent (L) of the first mask windows (32) and shallower than said lower boundary between the first mask windows.

15

6. A method of Claim 5 wherein the etchant etches the first mask material more slowly than the semiconductor body (2).

7. A method of manufacturing a vertical trench-gate transistor
20 semiconductor device of Claim 4 comprising the steps of etching grooves of uniform depth into the semiconductor body (2), and selectively etching portions of the grooves, such that the resulting trenches (6') are deeper than the lower boundary (100) of the channel-accommodating region (10) in the finished device within the lateral extent (L) of the source region stripes (8) and
25 shallower than said lower boundary between the source region stripes.

8. A method of manufacturing a vertical trench-gate transistor semiconductor device of any of Claims 1 to 3 having trenches (6) of substantially uniform depth, comprising the steps of forming a mask over the
30 top surface of the semiconductor body; and introducing dopant of the second conductivity type through the windows of the mask for the spaced regions (14).